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## **Report Title**

Quantum Information Processing Using Local Control of Exchange in 1D Nanotubes and Nanowires

#### **ABSTRACT**

The overall project aimed to develop gated nanotubes and nanowires to be used in the development of spin qubits arranged in a 1D array. Nanotube circuits with gate-confined single and double dots were realized, shell-core nanowire growth methods were developed, gated nanowire circuits were fabricated, and double quantum dots, appropriate for singlet-triplet qubits, were investigated experimentally. We also investigated light emission from nanowires, to be of potential use in electron-photon coupled qubits.

Theoretical work spanned the range from investigations of charge dephasing due to 1/f noise, quantum versus classical coupling to nuclear spins, and band mixing in graphene.

Dozens of papers were published, several patents were filed, and several students recieved PhD degrees as a result of this funding.

List of papers submitted or published that acknowledge ARO support during this reporting period. List the papers, including journal references, in the following categories:

(a) Papers published in peer-reviewed journals (N/A for none)

- J. Paaske, A. Rosch, P. Wolfle, N. Mason, C. M. Marcus and J. Nygard,
- "Non-equilibrium singlet-triplet Kondo effect in carbon nanotubes, Nature Physics 2, 460 (2006).
- M. J. Biercuk, D. J. Reilly, T. M. Buehler, V. C. Chan, J. M. Chow, R. G. Clark, C. M. Marcus, Charge Sensing in Carbon Nanotube Quantum Dots on Microsecond Timescales, (2005) Phys. Rev. B 73, 201402(R) (2006).
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Number of Papers published in peer-reviewed journals: 38.00
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Number of Non Peer-Reviewed Conference Proceeding publications (other than abstracts):
Peer-Reviewed Conference Proceeding publications (other than abstracts):
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(d) Manuscripts

Prof. Park:

- Y. Doh, K. N. Maher, L. Ouyang, J. Park, and H. Park, "Spatially resolved electroluminescence and photocurrent measurements from single-CdSe-nanowire optoelectronic devices," in preparation (2006)
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- Lara Faoro, J. Bergli, B.L. Altshuler and Yu.M. Galperin, "Models of environment and T\_1 relaxation in Josephson charge qubits", submitted to Phys. Rev. Lett.
- Emil A. Yuzbashyan, B.L. Altshuler, V.B. Kuznetsov and V.Z. Enolskii "Solution for the dynamics of the BCS and central spin problems", submitted to J. Phys. A
- Emil A. Yuzbashyan, Alexander A. Batine and B.L. Altshuler "Finite Size Corrections for the Pairing Hamiltonian", submitted to Phys. Rev. B

**Number of Manuscripts:** 8.00

### **Number of Inventions:**

#### **Graduate Students**

NAME Carl Barrelet	PERCENT_SUPPORTED 0.66	=
Jie Xiang	0.08	
Yongjie Hu		
0,	0.08	
Lian Ouyang	1.00	
Emil A. Yuzbashyan	0.50	
Gengfeng Zheng	1.00	) No
FTE Equivalent:	3.32	2
Total Number:	6	

## **Names of Post Doctorates**

<u>NAME</u>	PERCENT_SUPPORTED	
Dongmok Whang	1.00	No
Slaven Garaj	1.00	No
D.M. Basko	0.25	No
J. Bergli	0.25	No
FTE Equivalent:	2.50	
Total Number:	4	

<u>NAME</u>	PERCENT SUPPORTED	National Academy Member	
Charles M. Marcus	0.00	No	
Charles M. Lieber	0.00	No	
Hongkun Park	0.00	No	
Boris L. Altshuler	0.00	No	
FTE Equivalent:	0.00		
Total Number:	4		
	Names of Under Graduate st	udents supported	
<u>NAME</u>	PERCENT SUPPORTED		
FTE Equivalent:			
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	Names of Personnel receiving	g masters degrees	
NAME			
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	Names of personnel rec	eiving PHDs	
NAME			
Gengfeng Zheng	No		
Emil A. Yuzbashyan	No		
Lian Ouyang	No		
Total Number:	3		
	Names of other research	arch staff	
NAME	PERCENT SUPPORTED		
FTE Equivalent:			
Total Number:			

**Sub Contractors (DD882)** 

1 b. Office of Sponsored Research Accountin

New South Building, Seventh Floor

Princeton NJ 08544

**Sub Contractor Numbers (c):** 

Patent Clause Number (d-1):

Patent Date (d-2):

Work Description (e): Prof. Boris Altshuler, now of Columbia University, supprted our experimental efforts with a theoret

**Sub Contract Award Date (f-1):** 3/18/2002 12:00:00AM

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1 a. Columbia University

1 b. 722 West 168th Street

New York NY 10032

**Sub Contractor Numbers (c):** 

Patent Clause Number (d-1):

Patent Date (d-2):

Work Description (e): Prof. Boris L. Altshuler supported our experimental efforts with a theoretical analysis of dephasing

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1 a. Columbia University

1 b. 722 West 168th Street

New York NY 10032

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**Inventions (DD882)** 

# "Nanoscale Arrays, Robust Nanostructures, and Related Devices" Patent Filed in US? (5d-1) Patent Filed in Foreign Countries? (5d-2) Was the assignment forwarded to the contracting officer? (5e) N Foreign Countries of application (5g-2): 5a: C. M. Lieber, D. Whang, S. Jin, Y. Wu, M. McAlpine, and R. 5f-1a: Harvard University 5f-c: 1350 Massachusetts Avenue Cambridge MA 02138 "Nanowire Heterostructures" Patent Filed in US? (5d-1) Patent Filed in Foreign Countries? (5d-2) Was the assignment forwarded to the contracting officer? (5e) Ν Foreign Countries of application (5g-2): 5a: C. M. Lieber, W. Lu, J. Xiang, Y. Wu, B. P. Timko, H. Yan 5f-1a: Harvard University 5f-c: 1350 Massachusetts Avenue Cambridge MA 02138 "Nanowire Photonic Circuits, Components Thereof, and Related Methods" Patent Filed in US? (5d-1) Patent Filed in Foreign Countries? (5d-2) Was the assignment forwarded to the contracting officer? (5e) N Foreign Countries of application (5g-2): 5a: C. M. Lieber, C. J. Barrelet, and A. B. Greytak 5f-1a: Harvard University 5f-c: 1350 Massachusetts Avenue Cambridge MA 02138 Biercuk 2194: "Low Temperature Atomic Layer Deposition Liftoff Method for Microelectronics and Nanoelectronic Applications

Patent Filed in US? (5d-1) N

Patent Filed in Foreign Countries? (5d-2)

Was the assignment forwarded to the contracting officer? (5e) N Foreign Countries of application (5g-2):

5a: Michael Biercuk, Douwe Monsma, Charles M. Marcus, and R.

5f-1a: Harvard University

5f-c: 1350 Massachusetts Avenue

Cambridge MA 02138

# **Summary of Scientific Progress and Accomplishments**

Here we describe the overall research accomplishments group by group, with most recent work at the end.

Throughout the term of the grant, the goal of Marcus's research has been to fabricate gated quantum dot systems and to develop fast electrostatic gating and readout schemes that allow quantum dots formed along a carbon nanotube to function as a quantum-dot-based quantum computer. Two features make nanotubes attractive: 1) zero nuclear spin and weak spin orbit coupling suggest long spin coherence times; 2) small size makes quantization of energy levels relatively easily achieved, compared to GaAs devices. What has not been easy to do in nanotubes is to use gating to define quantum dots.

Once the group switched to Pd ohmic contacts, following the discovery by the Dai group that Pd makes good, p-type ohmic contacts [1], gate-depletable semiconducting tubes could be made readily, without requiring bending or kinking the tube (as was reported in Ref. [2]). This allowed us to fabricate and study double quantum dots, as an example [3].

This research lead us to a surprising discovery of fundamental physical interest: a gated single-wall carbon nanotube has conductance plateaus at integer multiples of e2/h, rather than the expected 2e2/h or 4e2/h. The lifting of degeneracy evident in these plateaus is not well understood but is probably related to the so-called "0.7 structure" in GaAs quantum point contacts [4].

In collaboration with the UNSW group, we next developed a fast charge readout scheme based on a proximal single-electron transistor (SET) fabricated adjacent to the carbon nanotube. This device provides fast readout of the charge state of a single gate-defined nanotube quantum dot [5].

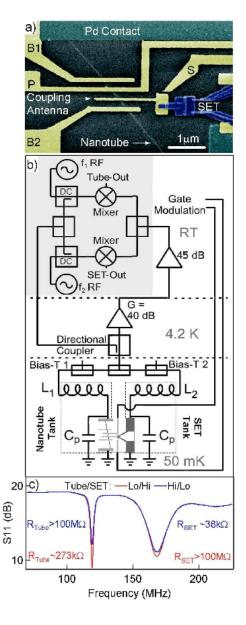


Fig. 1. (a) Single walled carbon nanotube with integrated SET charge detector. (b) Reflectometry circuit allowing microsecond readout of the charge state of the nanotube [5].

The work in Lieber's group has centered on the synthesis and transport studies of onedimensional germanium/silicon (Ge/Si) core/shell nanowire heterostructures. We have made substantial progress in this general area with (1) the synthesis and characterization of the nanowire system and (2) low-temperature transport studies of Ge/Si nanowire heterostructures.

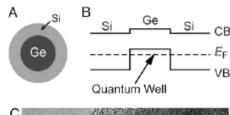
The Ge/Si core/shell (Fig. 2A) nanowires were grown using previously developed approach, except that both the Ge core and Si shell were not doped. This difference is critical for our studies since it eliminates scattering from ionized dopants in the 2-5 nm thick Si shell adjacent to the Ge channel. A thin Si shell was used in our studies to facilitate electrical contact to the Ge channel, and to reduce the likelihood of dislocations in the shell. The valence band offset of

ca. 500 meV between Ge and Si at the heterostructure interface serves as a confinement potential

for the quantum well, and free holes will accumulate in the Ge channel when the Fermi level lies below the valance band edge of the Ge core (Fig. 2B). High-resolution transmission electron microscopy studies of the Ge/Si nanowires (Fig. 2C) show clearly the core (dark)/shell (light) structure. The lattice fringes and sharp interface between Ge and Si show that the core/shell structure is epitaxial, and is consistent with cross-sectional elemental mapping results. Lower resolution images also indicate that dislocations are not present in these structures. The clean, epitaxial interface in these nanowire heterostructures should produce a smooth confinement potential along the channel.

Electrical transport measurements were made on Ge/Si nanowire devices with lithographically-patterned nickel source/drain electrodes and capacitively coupled back-gate electrodes. A brief annealing process was performed after the source/drain fabrication to facilitate contact to the inner Ge channel. Room-temperature current versus source-drain voltage  $(I-V_{\rm SD})$  data recorded on a het-

erostructure with a 10 nm Ge core diameter (Fig. 3A) exhibit a substantial current at zero gate voltage ( $V_g = 0$ ), and a decrease in current as  $V_g$  is increased from -10 to 10 V. These results show that the device behaves as a ptype depletion mode field-effect transistor (p-FET), and thus confirm the accumulation of hole charge carriers. Because both the Ge



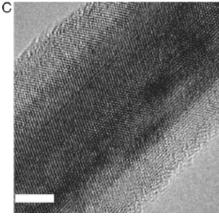


Fig. 2 Core-shell Si/Ge nanowire

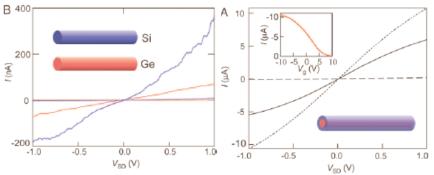


Fig. 3 Current-voltage characteristics of Si, Ge, and Si/Ge nanowire.

core and the Si shell are un-doped, the existence of a hole gas is a result of the band line-up as illustrated in Fig. 2B, where the Fermi level is pinned below the Ge valance band edge, due to the combined effect of work function, band offset and interface states. In contrast, experiments on intrinsic Si (i-Si) and intrinsic Ge (i-Ge) nanowires (Fig. 3B) show that both the i-Si and i-Ge nanowires are enhancement mode p-FETs with no carriers at  $V_g$ =0. The i-Ge nanowire data thus contrast that obtained for the Ge/Si core/shell structure even though the i-Ge nanowires were grown under identical conditions to the Ge core in the heterostructure.

In single component semiconductor nanowire devices, a Schottky barrier always forms at the contact since the Fermi level ( $E_{\rm F}$ ) lies inside the semiconductor band gap. In contrast, barriers to the hole gas in Ge/Si nanowires are not intrinsic and can be eliminated, since  $E_{\rm F}$  lies outside the Ge bandgap (Fig. 2B). Indeed, annealing the Ge/Si nanowire devices produces reproducible transparent contacts to the hole gas even at low temperatures. I- $V_{\rm SD}$  data obtained at 4.7 K on an annealed device with a 10 nm core (Fig. 4A, inset) close to depletion ( $V_{\rm g}$  = 10 V) are linear around  $V_{\rm SD}$  = 0, and thus show that the contacts are transparent at low temperatures. At small

bias the I-V<sub>SD</sub> curves collapse for V<sub>g</sub> < 7 V (right inset, Fig. 4A). This behavior is highlighted by plotting G vs.  $V_g$  (Fig. 3A), where G first rises sharply and then plateaus for  $V_{\rm g}$  < 7 V. The plateau conductance,  $\sim 50 \mu S$ , is 0.65 of  $2e^2/h$ , the value expected for a spin-degenerate single-mode ballistic conductor. Variations in the plateau conductance are suggestive of Fabry-Perot interferences, but are not quantified here due to their small amplitude. Studies of additional devices show very similar results and highlight the reproducible transport properties of the Ge/ Si nanowire system. For example, Fig. 4B shows G vs.  $V_{\rm g}$  recorded at different temperatures for another 10 nm core diameter device. At 4.7 K, the device shows a conductance plateau close to  $2e^2/h$ , which is consistent with data in Fig. 4A and the value for a single-mode ballistic conductor. Notably, increasing temperature up to 300 K yields little change in the value of the conductance plateau, although the slope becomes somewhat smeared. This fact implies that even at room temperature only a single 1D subband participates in transport and that the mean free path exceeds the channel length of 170 nm; that is, transport through the Ge/Si nanowire remains ballistic up to at least this length scale.

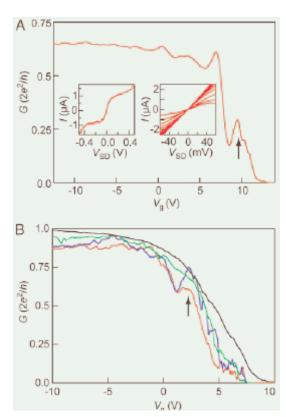


Fig. 4 Gate Dependent conductance of a Si/Ge nanowire.

In addition, the Lieber group has studied devices with a top-gate structure, which increases the gate coupling, in order to probe transport through more than one subband. G- $V_g$  data recorded on a 400 nm long device (Fig. 5A) shows four distinct conductance plateaus at 5 K. We attribute these plateaus to transport through the first four subbands in the Ge/Si nanowire, and confirmed this assignment by plotting G- $V_{SD}$  for different values of  $V_g$  (Fig. 4B). In this plot, the conductance plateaus appear as dark regions, labeled as a-d, where several G- $V_{SD}$  curves at different  $V_g$  overlap, since  $V_g$  does not affect G in the plateau regions. At large  $V_{SD}$  these integer plateaus evolve into "half" plateaus (f-g) when the source and drain chemical potentials cross different subbands. For example, the 0.5 plateau, appearing as the dark region labeled f, corresponds to the case where the source potential drops below the first subband bottom while the drain poten-

tial still lies above it. Similarly, feature g corresponds to the 1.5 plateau, which evolves from the second (b) and first (a) subbands. The small cusp feature near zero-bias in the G- $V_{\rm SD}$  data is due to shallow potential barriers with heights of a few meV. The assignment of these features to 1D subbands in the Ge/Si nanowires was further analyzed by quantifying the level spacings. Such features appear more pronounced after numerically differentiating G against  $V_g$ . A plot of the transconductance,  $dG/dV_g$ , as a function of  $V_{\rm SD}$  and  $V_{\rm g}$  (Fig. 5C) shows zero or low values at conductance plateaus and high values in the transition regions between plateaus, which are highlighted by dashed lines in the fig-The subband spacings are obtained directly from these data as the  $V_{\rm SD}$  values at the apexes of

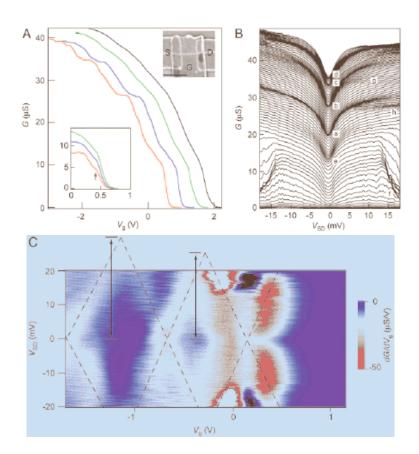


Fig. 5 Gate dependent conductance shows 0.7-like features.

the full plateaus (i.e., the extrapolated intersections of the dashed lines), which yield  $\Delta E_{1,2} = 25$  mV and  $\Delta E_{2,3} = 30$  mV. For comparison, we have calculated the subband spacings using an effective mass model with a cylindrical confinement potential with radius r to approximate the Ge/Si nanowire structure. The energy levels of the 1D modes due to radial confinement are

$$E = \frac{\hbar^2 u_{ni}^2}{2m^* r^2}$$

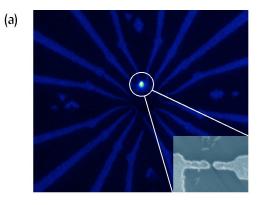
where  $u_{ni}$  is Bessel function's  $J_n(x)$ 's i<sup>th</sup> zero point, and  $m^*$  is the hole effective mass as discussed above. For a nanowire with 14 nm Ge core diameter, we obtain  $\Delta E_{1,2} = 25$  mV and  $\Delta E_{2,3} = 32$  mV. These values are in good agreement with our experimental data (Fig. 4C), and thus provide strong support for our assignment of discrete 1D subbands in the Ge/Si nanowire heterostructures.

A reproducible feature was observed with a conductance value ~0.7 times the first plateau in the bottom-gated (Fig. 5, vertical arrows) and top-gated (Fig. 4A, inset; Fig. 4B, label-*e*) devices. Similar features, termed "0.7 structure", have been observed previously on quantum point contacts and quantum wires formed in clean 2DEG samples. This feature is generally believed to

be caused by spontaneous spin polarization in low-dimensional interacting electron gas systems due to the formation of a spin gap or a localized spin. Temperature dependent data recorded on a back-gated Ge/Si device (Fig. 5B) show that the 0.7 feature initially increases in magnitude and then broadens as temperature is increased to 50 K, consistent with the spin-gap hypothesis. These results suggest that the "0.7 structure" is not restricted to electron gas samples, but a universal phenomenon in 1D systems. In this regard, the heavier effective mass of holes in the Ge/Si nanowires compared to electrons will yield a larger interaction parameter, and should make Ge/Si nanowires interesting to study in greater detail in the future.

During this grant, the Park group investigated coupled charge transport, electroluminesphotoconductivity cence. singlenanostructure transistors that incorporate individual CdSe nanocrystals and CdSe/CdS nanowire heterostructures. In the first study, we have fabricated and characterized light-emitting transistors incorporating individual CdSe nanocrystals (see Fig. 1(a)). Electrical measurements conducted at low bias voltage and low temperature show clear evidence of Coulomb blockade behavior, indicating that electrons pass through the nanocrystal by single-electron tunneling. Once the bias voltage exceeds the band gap of CdSe, devices with asymmetric tunnel barriers emit linearly polarized light. Combined analyses of the electrical and optical data indicate that the tunnel couplings between the nanorod and the metallic electrodes change significantly as a function of bias voltage and that the light emission results from the inelastic scattering of tunneling electrons.

The Park group has also developed a method to synthesize CdSe/CdS nanowire heterostructures using a metal-catalyzed liquid-solid synthesis. These nanowire heterostructures could not be prepared using a more conventional vapor-liquid-solid (VLS) method because CdSe and CdS tend to alloy at high temperatures ( $> 700^{\circ}$ C) required for the VLS synthesis. The new solution-phase synthesis scheme that we developed allows the synthesis of long ( $> 5 \mu m$ ), single-crystalline nanowire heterostructures at much lower temperatures ( $< 250^{\circ}$ C), thereby enabling the preparation of nanowire heterostructures with well de-





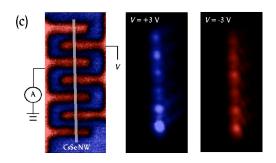


Fig. 6. (a) An optical micrograph of a light-emitting transistor incorporating individual CdSe nanocrystals. The inset shows an SEM image of the device. (b) An SEM image of a CdS/CdSe/CdS nanowire heterostructure. (c) Left: An optical micrograph of a device incorporating a single CdSe nanowire. Right: Scanning photoconductivity plots of the same device obtained at two different bias voltages.

fined boundaries between nanowire sections with distinct chemical composition (see Fig. 6(b)).

The Park Group has also fabricated devices incorporating these nanowire heterostructures and started to investigate their charge transport, electroluminescence, and photoconductivity properties. These studies show that electroluminescence in CdSe-nanowire devices occurs at the nanowire/electrode junction where holes are injected, whereas the photoconductivity enhancement is strongest at the junction where electrons are injected (see Fig. 6(c)). The information gained in this study will play a crucial role in realizing nanowire-heterostructure-based turnstile devices that can act as a single-photon on-demand source.

Recently, Marcus and Lieber have jointly investigated gate-defined multiple quantum dot systems in Si/Ge shell-core nanowires, confined with lithographically patterned gates. The insulation between gate and nanowire is the high-k dielectric HfO<sub>2</sub>, deposited by atomic layer deposition (ALD). Nanowires offer great promise for solid-state quantum information processing using spin-based physical qubits due to weak spin-orbit coupling and low concentrations of nonzero-spin nuclei. In contrast, spin qubits in GaAs are subject to rapid dephasing due to hyperfine and spin orbit effects. The effort toward nanowires complements our work in carbon nanotubes, which shares with the Si/Ge nanowires these two advantages. A micrograph of one of the devices is shown in Fig. 7. An important component of the device is an integrated charge sensor, which allows the charge state of the double quantum dot to be read out without requiring transport through the device to measured, or even measurable. This work is being prepared for publication.

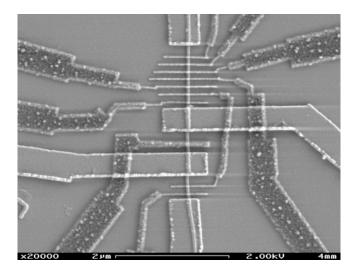


Fig. 7. Micrograph of a Si/Ge nanowire double quantum dot with integrated charge sensor. The nanowire runs top to bottom. The upper region is the double dot (with seven gates defining dot regions). The lower region is the sensor, electrostatically coupled to the upper region via a coupling gate in the form of a backward "C".

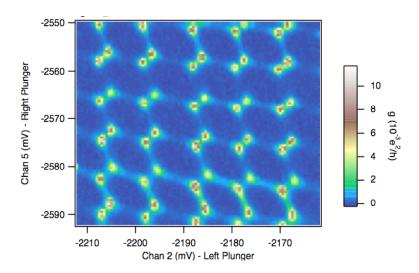


Fig. 8. Conductance of a nanowire double quantum dot as a function of gate voltages on two of the gates. The familiar "honeycomb" of conductance shows charge occupancy states of the double dot, quantized due to the Coulomb blockade. These measurements were carried out at  $\sim 100 \text{mK}$ .

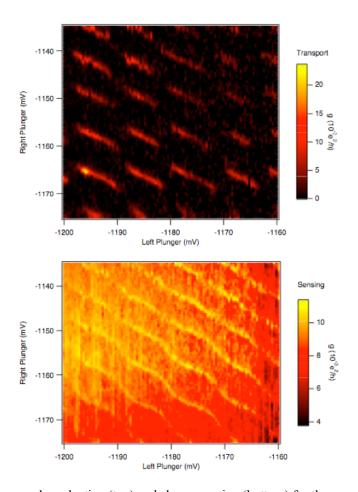


Fig. 9. Simultaneously measured conduction (top) and charge sensing (bottom) for the nanowire double quantum dot at 100mK. These data were from a regime with strong inter-dot tunneling.

In addition, the Marcus group has continued to develop nanotube-based multiple quantum dots. We have changed our method of insulation from using ALD (which doped the nanotubes chemically) to using controlled oxidation of aluminum gates. This method was developed by the Kouwenhoven Lab in Delft to produce gated nanotubes [6, 7]. They generously shared the recipe with us.

The effects of surface roughness double layer graphene-based electronics has been investigated theoretically by Altshuler and collaborators [8]. Double layer graphene may be better suited for gating because of the gap induced by the coupling between layers. During this period, Altshuler also investigated hyperfine coupling of electrons in a double quantum dot [9], showing an important distinction between quantum and classical behavior of the nuclear ensemble. These results can be tested in the <sup>13</sup>C nanotubes currently being fabricated.

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